High-Performance *W*-Band Monolithic Pseudomorphic InGaAs HEMT LNA's and Design/Analysis Methodology

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Abstract—**High-performance *W*-band monolithic one- and two-stage low noise amplifiers (LNA's) based on pseudomorphic InGaAs/GaAs HEMT devices have been developed. The one-stage amplifier has a measured noise figure of 5.1 dB with an associated gain of 7 dB from 92 to 95 GHz, and the two-stage amplifier has a measured small signal gain of 13.3 dB at 94 GHz and 17 dB at 89 GHz with a noise figure of 5.5 dB from 91 to 95 GHz. An eight-stage LNA built by cascading four of these monolithic two-stage LNA chips demonstrates 49 dB gain and 6.5 dB noise figure at 94 GHz. A rigorous analysis procedure was incorporated in the design, including accurate active device modeling and full-wave EM analysis of passive structures. The first pass success of these LNA chip designs indicates the importance of a rigorous design/analysis methodology in the millimeter wave monolithic IC development.**

I. Introduction

MONOLITHIC millimeter-wave integrated circuits provide significant advantages of small size, repeatability and low cost at high volume over the conventional hybrid integrated circuit components in millimeter wave radar, electronic warfare, smart weapon, and radiometer system applications. The low noise amplifier (LNA) is a key component in the receiving portion of these systems. The motivation of this work was to achieve state-of-the-art performance of a monolithic LNA in *W*-band to improve the performance of existing systems and enable new applications. A successfully developed *W*-band monolithic downconverter [9] and an eight-stage high gain amplifier prove the feasibility of the monolithic LNA approach.

W-band monolithic one- and two-stage LNA's have been designed, fabricated and tested with demonstrated excellent performance. For the one-stage LNA, a noise figure of 5.1 dB with 7 dB associated gain from 92 to 95 GHz has been measured, while the two-stage LNA shows 13.3 dB gain at 94 GHz, 17 dB gain at 89 GHz and 5.5 dB noise figure from 91 to 95 GHz. The results of the two-stage LNA not only are the best monolithic LNA performance at *W*-band frequency reported to date [1]–[5], but also rival some recently reported hybrid LNA results [6]. Table I compares the present work [10] with previously published results [1]–[6]. An eight-stage LNA built by cascading four of these monolithic two-stage LNA chips demonstrates 49 dB gain and 6.5 dB noise figure at 94 GHz, which is the highest gain unit ever achieved at this frequency. Moreover, the first monolithic *W*-band downconverter has also been successfully developed using a similarly designed LNA followed by a singly balanced HEMT gate diode mixer [9].

A rigorous design/analysis procedure was developed for these *W*-band monolithic LNA's. This procedure includes accurate HEMT device modeling and full-wave electromagnetic (EM) analysis for the passive structures. In fact, the methodology is applicable for all monolithic millimeter-wave integrated circuit (MMWIC) designs. The first pass success of this LNA chip design indicates the importance of a rigorous design/analysis methodology for millimeter-wave monolithic IC development. This design/analysis procedure is described from Section II to IV along with device characteristics and circuit design considerations. Section II presents the characteristics of the InGaAs pseudomorphic (PM) HEMT's used in the LNA's and the accurate modeling technique. Full-wave EM analysis of passive structures is described in Section III. The design considerations of *W*-band monolithic LNAs and the design/analysis methodology are discussed in the Section IV. Section V shows the performance of the one- and two-stage LNA's, and test results of an eight-stage LNA built by cascading four monolithic two-stage LNA chips. A brief summary is given in Section VI.

II. PM HEMT Characteristics and Device Modeling

A. PM HEMT Characteristics

The devices reported in this paper have been optimized for high gain operation at *W*-band. The InGaAs PM HEMT uses a planar doping layer to achieve high channel

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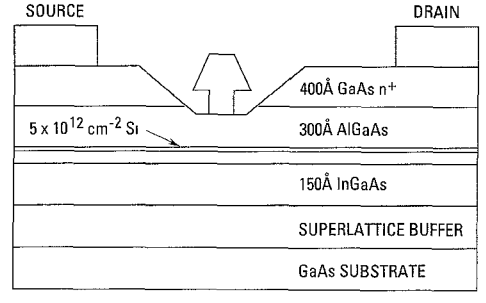
TABLE I
PERFORMANCE SUMMARY OF LNA'S AT *W*-BAND

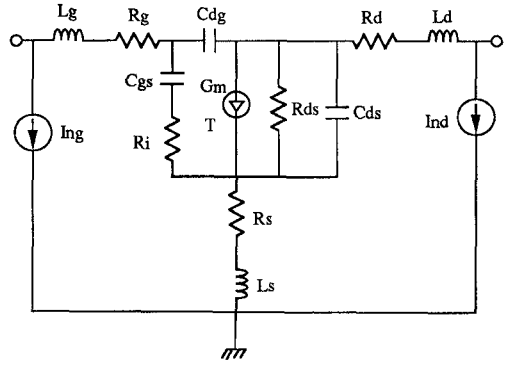
Device Technology	No. of Devices	Gain/NF (dB) @ 94 GHz	LNA Design Features
GaAs-based PM HEMT	1	5.0/NA	MMIC one-stage [1]
GaAs-based PM HEMT	1	5.0/NA	MMIC one-stage [2]
InP-based HEMT	2	8.0/NA	MMIC cascode configuration [3]
InP-based HEMT	5	6.0/NA	MMIC distributed amplifier [4]
InP-based HEMT	7	6.0/NA	MMIC distributed amplifier [5]
GaAs-based PM HEMT	2	9.7/4.2	Hybrid [6]
InP-based HEMT	2	11.5/3.3	Hybrid [6]
GaAs-based PM HEMT	2	13.3/5.5	MMIC two-stage, present work [10]
GaAs-based PM HEMT	8	49/6.5	Eight-stage, present work [15]

aspect ratio as well as higher electron transfer efficiency for higher transconductance. The device and MMIC fabrication process used for this work has been previously reported [8]. A cross-section of the HEMT is shown in Fig. 1(a). The 0.1 μm T-gate InGaAs PM HEMT's fabricated using this process typically have a dc transconductance (G_m) of 670 mS/mm with a cut-off frequency (f_t) of 130 GHz, which is as high as the devices with a conventional trapezoidal cross section gate. Compared to the device with a conventional gate structure, the noise performance of the T-gate PM HEMT is improved owing to the lower gate resistance.

In the LNA design, a four-finger, 40 μm gate periphery HEMT was used in both one- and two-stage amplifiers. The linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal *S*-parameters to 40 GHz. Noise model parameters used for simulation are obtained from fitting measured noise parameters to 26 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters. The circuit model parameters of the device at 2 V drain voltage and the peak transconductance (g_m) condition are shown in Fig. 1(b). The accurate device measurement and modeling techniques are discussed as follows.



(a)



T (sec)	Cdg (fF)	Cgs (fF)	Cds (fF)	gm (ms)	Rds (ohm)	Ri (ohm)	Rg (ohm)	Rs (ohm)	Rd (ohm)	Lg (pH)	Ls (pH)	Ld (pH)
0.4	7.7	27	19	28	531	1.4	2.3	3.0	3.7	1.1	1.0	1.3

(b)

Fig. 1. The InGaAs PM HEMT structure and equivalent circuit model. (a) The InGaAs PM HEMT profile. (b) The linear small signal equivalent circuit and noise model of 40 μm HEMT.

B. Accurate Device Modeling

The accuracy of device models relies heavily on the precise measurement of discrete devices. Since the on-wafer measurement is not available in *W*-band at the present time, a frequency extrapolation model obtained from the low frequency *S*-parameters measurement becomes inevitable. Errors in measurement of the low frequency *S*-parameters (typically 1–26 GHz or 1–40 GHz) will significantly affect the behavior of the model at 94 GHz. The commercial calibration standards, e.g., open, short, load and through, usually generate uncertainties during the calibration procedure. These calibration uncertainties are ascribed to the discontinuities of the co-planar ground-signal-ground line probe launcher, the vague definition of the calibration reference planes at the probing positions and the inexact open end capacitance of the probe tips, etc. The measurement inaccuracy caused by these uncertainties becomes worse for a smaller device required to operate at a higher frequency. For example, the open end capacitance of the probe is in the order of 5–10 fF, while the C_{gs} of a 40 μm HEMT device used in the amplifiers is around 25 fF. The percentage error can be as high as 20% and causes significant change of frequency response at *W*-band.

In order to overcome these ambiguities, a set of specially designed on-wafer calibration standards was constructed on the same wafer along with the monolithic LNA's and discrete devices. Fig. 2(a) shows the layout

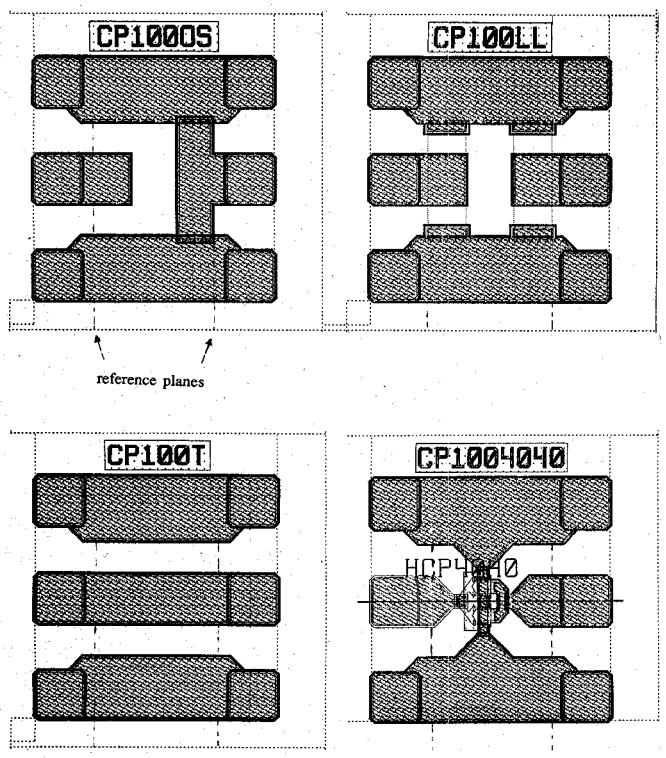


Fig. 2. Layouts of the on-wafer calibration standards and discrete HEMT device.

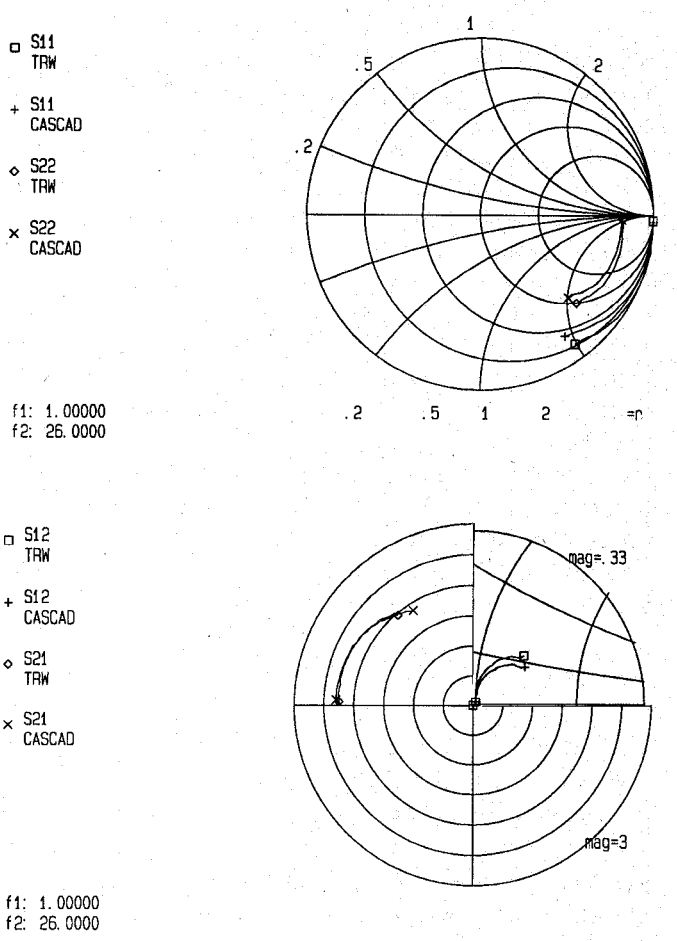


Fig. 3. Comparison of *S*-parameters measurement for 40 μm HEMT obtained from conventional calibration standards (CASCAD) and newly developed ones (TRW).

for this set of calibration standards and the 40 μm discrete HEMT device. The calibration standards consist of coplanar wave-guide (CPW) open, short, load and through which have the same feed patterns as the device to be tested. These standards are modeled carefully with full-wave EM analysis [7] and the reference planes are clearly defined at a special location from the edge of probe pads as indicated in the layouts. The models of these standards can be entered in the calibration kit of HP8510 network analyzer to perform the *S*-parameter measurement. Fig. 3 compares the measured small signal *S*-parameters of a 40 μm InGaAs PM HEMT at 2 V drain bias with gate biased on g_m peak using the Cascade impedance substrate and the on-wafer CPW calibration standards. It is observed that the measured S_{11} trace follows a higher constant resistance circle when using the Cascade calibration standards. This results in higher R_g in the small signal model and causes a significant underestimation of the device's gain at high frequency. The maximum available gain of two models derived from these two sets of measurement data has a difference of about 3 dB at 94 GHz.

III. Passive Structure Analysis

A. Full-Wave EM Analysis of Passive Structures

There are some problems with present passive structure models between *W*-band and microwave frequency in the monolithic integrated circuits design. The validity of models, which are generated by quasi-static analysis or empirical formula [13], [14] and widely used in most microwave circuit theory based computer aided-design (CAD) programs, should be further investigated. Also, microwave circuit theory should be applied carefully since the coupling effect between elements tends to be stronger at high frequencies. The numerical full-wave EM analysis to characterize arbitrarily shaped MMIC structures becomes important to overcome these problems.

Several full-wave EM analysis tools are commercially available based on different approaches using different physical assumptions or numerical techniques. These approaches include method of moment to solve various integral equations and finite element method to solve partial different equations (Maxwell's equations). Based on the obtained surface current or field distribution, any particular passive MMIC structures can be characterized in terms of the *S*-parameters which is suitable for circuit design. The EM analysis being used in our design is a method of moment solution for the surface current integral equation based on the assumption of stratified medium in a conducting box [7].

B. Concerns of Full-Wave EM Analysis

The accuracy of numerical solutions in the full-wave EM analysis is always a concern. The convergence and consistence of the numerical solutions for such analyses

are not guaranteed in general unless they have been proved. This task is usually difficult since the Helmholtz operator from frequency domain Maxwell's equations is indefinite instead of positive-definite under most of boundary conditions. Thus each solution of the full-wave EM analysis should be investigated carefully and ensured to be meaningful before being used in the design. Sometimes, the numerical solution of current distributions are clues for judgement. An example will be given later.

The computation time is another issue of full-wave EM analysis in the design cycle since such analysis is a CPU intensive job for computers. Currently, most microwave circuit theory based CAD tools allow optimization to fine tune the circuit performance. However, optimization of circuit performance using EM analysis is not practical for the time being. In order to use the tools more efficiently, a design/analysis procedure is developed in our *W*-band monolithic IC design. This procedure is described in Section IV-B.

IV. Circuit Design Considerations and Design Methodology

A. W-Band LNA Design Considerations

Fig. 4(a)–(d) shows the circuit schematic diagrams as well as photographs of the complete monolithic one- and two-stage LNA's. These circuits are designed based on conventional reactive matching techniques using quasi-low pass topologies to achieve the maximum gain. All the matching networks are realized with microstrip lines on a 100 μm thick GaAs substrate. Edge-coupled lines are used for dc blocking in the two-stage design and radial stubs are employed for RF by-pass. N^+ bulk resistors are used in bias network to ensure stability of the amplifiers, and reactive ion etching (RIE) technique is applied to fabricate back-side via holes for grounding and dc returns. The chip size of one- and two-stage LNA's are 1.3×1.2 mm^2 and 2.2×1.2 mm^2, respectively.

The present LNA designs eliminate the use of metal-insulator-metal (MIM) capacitors and thin-film resistors (TFR's) which are employed in most of other MMIC designs. The elimination of these components saves two process steps (nitride deposition for MIM capacitors and resistive thin film deposition for TFR), providing improved yield and lower the cost of the chip fabrication without TFR and MIM variations. Typically, they are 15–30% from the nominal values of the capacitance and resistance. Moreover, the risks of degrading the HEMT performance during these two process steps and the modeling uncertainty of the MIM capacitors, for which no experimentally verified models at this frequency have been reported to date, are avoided. A large on-chip shunt MIM capacitor is often included in the bias network for low frequency by-passing and stability in millimeter-wave LNA designs [11], [12]. To insure stability without large on-chip by-pass capacitors, a shunt resistor of 150 Ω is added to drain bias network and 50 Ω to gate bias network. These resistors cause an additional dc current consumption of 20 mA for each stage when biased at 3 V. Although this design approach does not require the TFR or MIM capacitor process steps, all MMIC's reported here were subjected to the complete MMIC process since some other circuits on the mask required these additional components.

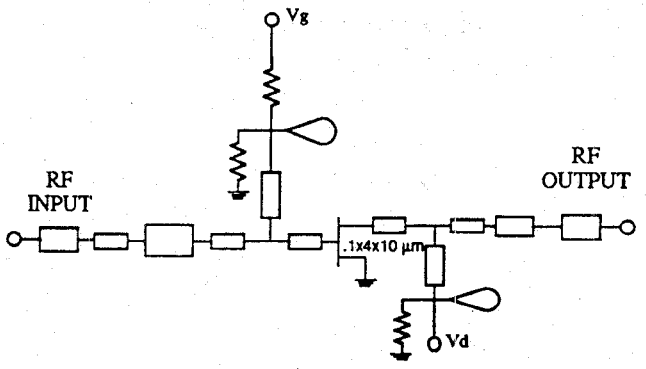
B. Rigorous Design/Analysis Procedure

A flow chart depicting the design/analysis procedure for our monolithic *W*-band LNA development is shown in Fig. 5. The *W*-band monolithic two-stage LNA is used as an example to illustrate this design/analysis procedure. After careful device modeling as described in Section II-B has been complete, conventional circuit synthesis and simulation using existing models of passive elements should be performed for the initial design. In this two-stage LNA case, the quasi-low pass filter structures are used for matching network, edge-coupled lines are selected to block dc voltage and radial stubs are chosen as RF ground for our two-stage design. Next, the critical components for which the models are suspected to be inaccurate so as to affect the circuit performance at *W*-band need to be identified and characterized by EM analysis. The edge coupled line and radial stub were analyzed in this design exercise. Significant discrepancies can be observed between the conventional quasi-static and full-wave analyses as shown in Fig. 6(a)–(b). Both the insertion loss of the edge-coupled line and the reflection coefficient of the radial stub show 10–20 degrees phase differences between the two models.

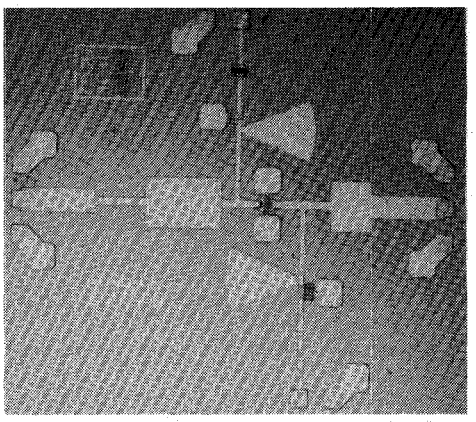
To judge whether the EM analysis gives reasonable answer, the current distribution of the edge-coupled line obtained from the numerical calculation is illustrated in Fig. 7(a)–(b) as an example. The magnitude of current distribution on the edges is in proportion to the darkness in the figures. Fig. 7(a) is the current distribution excited at 90 GHz. The distribution is almost symmetrical and the energy is strongly coupled. This is consistent with the designed coupled pass band centered around 94 GHz. On the other hand, Fig. 7(b) shows that when this structure is excited by a stop band frequency of 60 GHz. The current density at the output edge is much lower than that at the input edge and is not uniformly distributed along the transverse direction, which implies only little energy is coupled through the coupled line. This provides evidence for validity of the EM analysis from the view point of physical meaning.

The design is then modified based on resimulation using the EM analysis results. After the design is complete, the entire matching structures should be analyzed by EM theory to ensure no severe coupling effects between elements. If there is significant impact on the circuit performance, one needs to redefine more complicated critical components and repeat the analysis and design procedure.

The linear simulation results of the two-stage *W*-band LNA based on our design/analysis methodology and the conventional procedures are shown in Fig. 8. There are



(a)



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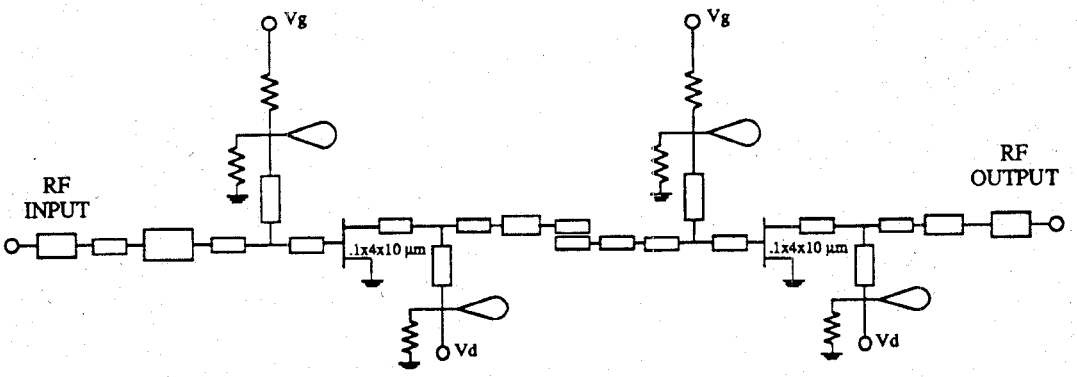
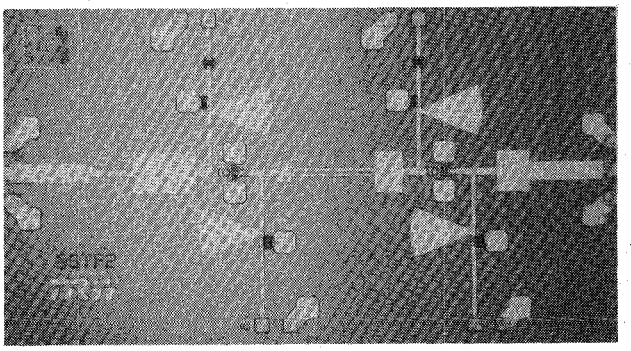


(c)



(d)

Fig. 4. Schematic diagrams and photographs of the *W*-band one- and two-stage MMIC LNAs. (a) One-stage LNA schematic diagram. (b) Photograph of the one-stage LNA. (c) Two-stage LNA schematic diagram. (d) Photograph of the two-stage LNA.

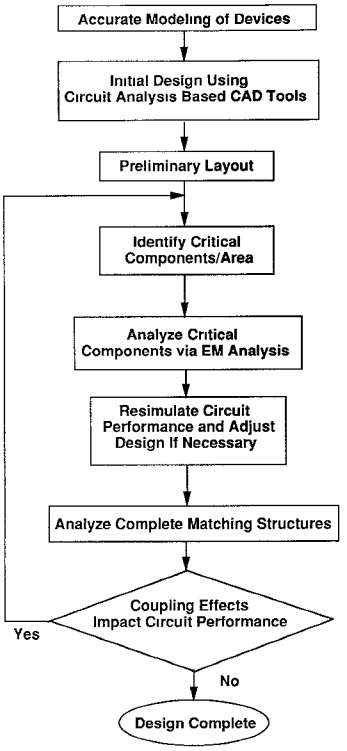
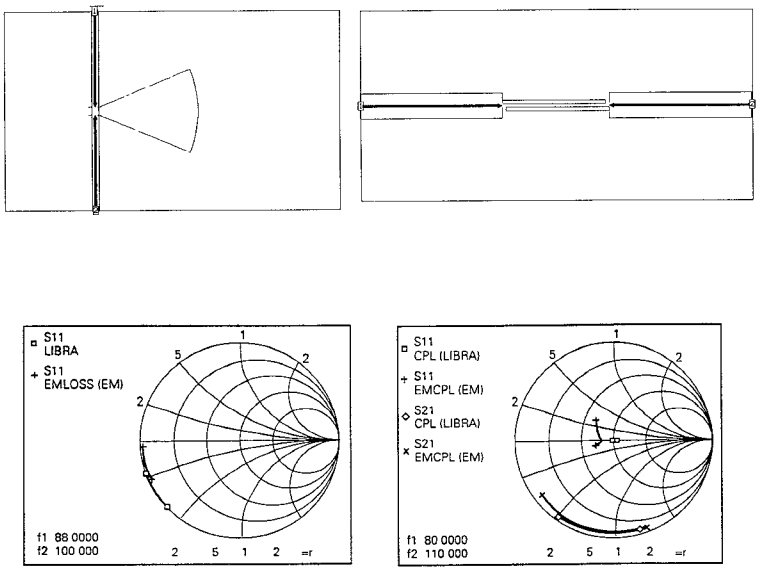


Fig. 5. Flow chart to illustrate the rigorous design/analysis methodology.



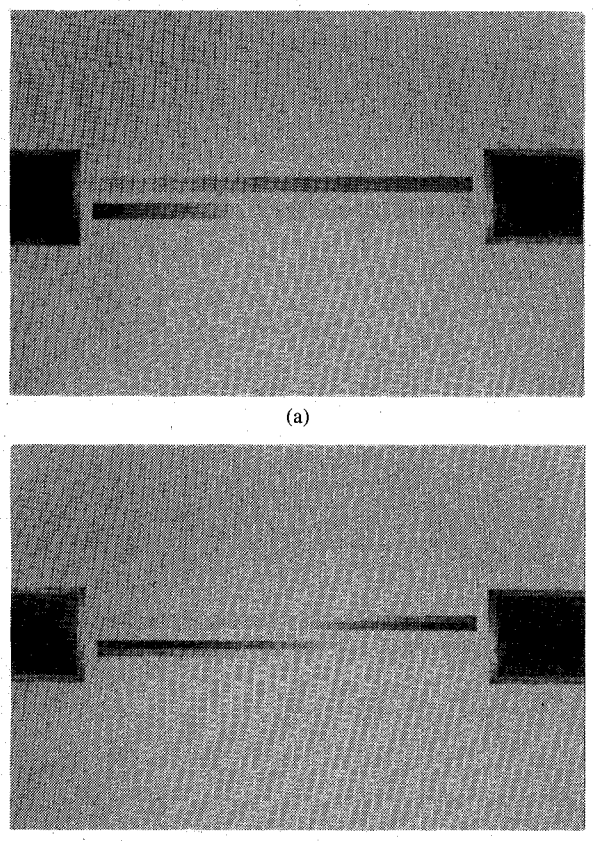
(a) (b)

Fig. 6. Comparison of S-parameters analyzed via full-wave EM theory (EM) and quasi-static assumption (LIBRA). (a) Radial stub. (b) Edge-coupled lines.

significant differences between these two results at W-band. The comparison of simulation results with measurement will be presented in the Section V-B.

V. LNA Performance

Both one- and two-stage LNA circuits were measured in a WR10 waveguide test fixture. Anti-podal finline transitions on 125 μm thick fused silica substrate are used to couple the signal from waveguide to microstrip. Fig. 9(a) shows the photograph of the waveguide to microstrip transition test fixture. The insertion loss of this transition fixture with a back-to-back transition connection is 1.7 to 2.0 dB from 88 to 96 GHz as shown in Fig. 9(b). All the measurement LNA results described below were corrected assuming half the back-to-back insertion loss is attributable separately to the input and output of the device under test.



(a)

(b)

Fig. 7. Surface element distribution of the edge-coupled lines obtained from full-wave EM analysis at (a) 90 GHz. (b) 60 GHz. The magnitude of current distribution on the edges is proportional to the darkness in the figures.

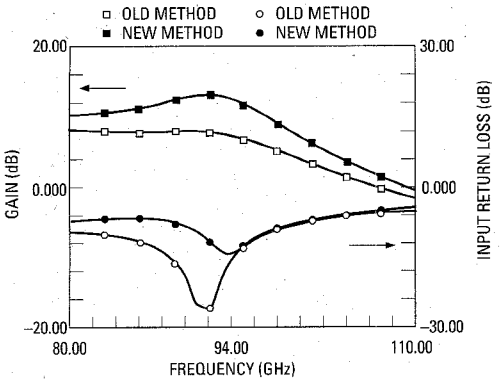
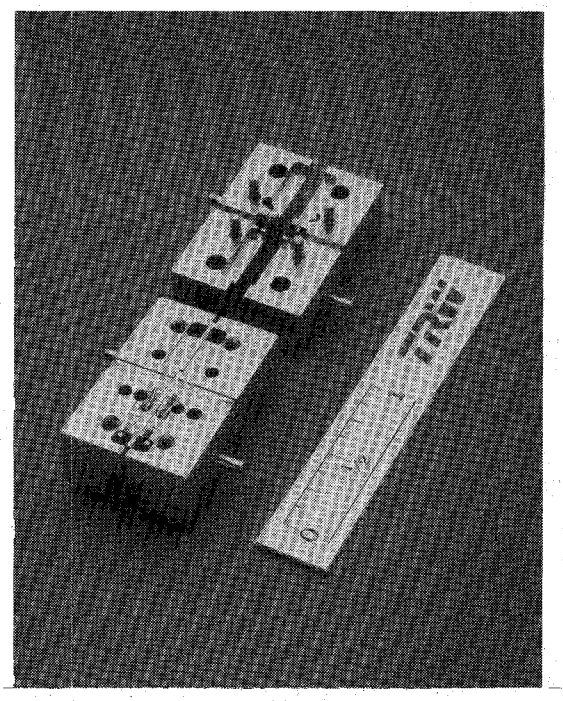


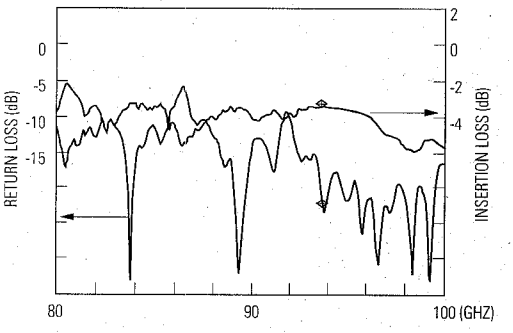
Fig. 8. Comparison of the simulated *W*-band two-stage LNA performance using conventional design approach (OLDMETHOD) and our design/analysis methodology (NEWMETHOD).

A. Monolithic One-Stage Amplifier Results

The measured data of the one-stage LNA under 3 V drain voltage and gate biased near g_m peak condition are presented in Fig. 10(a)–(c). The noise figure and associated small-signal gain performances from 92 to 95 GHz are shown in Fig. 10(a), which demonstrate a gain of 7 dB and a noise figure of 5.1 dB at 94 GHz. Fig. 10(b) illustrates the input return loss and uncorrected gain. The input return loss is better than 10 dB. Output return loss is better than 7 dB as shown in Fig. 10(c).



(a)



(b)

Fig. 9. Photograph and measurement results of the *W*-band test fixture and finline transition. (a) Photograph of the complete test fixture. (b) Insertion loss and return loss of the finline transition.

B. Two-Stage Amplifier Measurements and Comparison with Simulations

The measured data of the two-stage LNA are presented in Fig. 11(a)–(d). The noise figure and associated small signal gain performances from 91 to 95 GHz are shown in Fig. 11(a), which demonstrate a gain of 13.3 dB and a noise figure of 5.5 dB at 94 GHz. Fig. 11(b) illustrates the input return loss and uncorrected gain from 80 to 100 GHz. The input return loss is better than 10 dB from 91 to 97 GHz. At 89 GHz, the measured gain including fixture loss is 15.3 dB or 17 dB after correction. Output return loss is better than 5 dB across the 80 to 100 GHz band as shown in Fig. 11(c). The input power versus output power plot is shown in Fig. 11(d). The output 1 dB compression point of this LNA is 4 dBm and the two-tone output third-order intermodulation intercept point (IP3) is 13 dBm. All of results presented above are under 3 V drain bias condition with gate voltage near peak g_m for both stages.

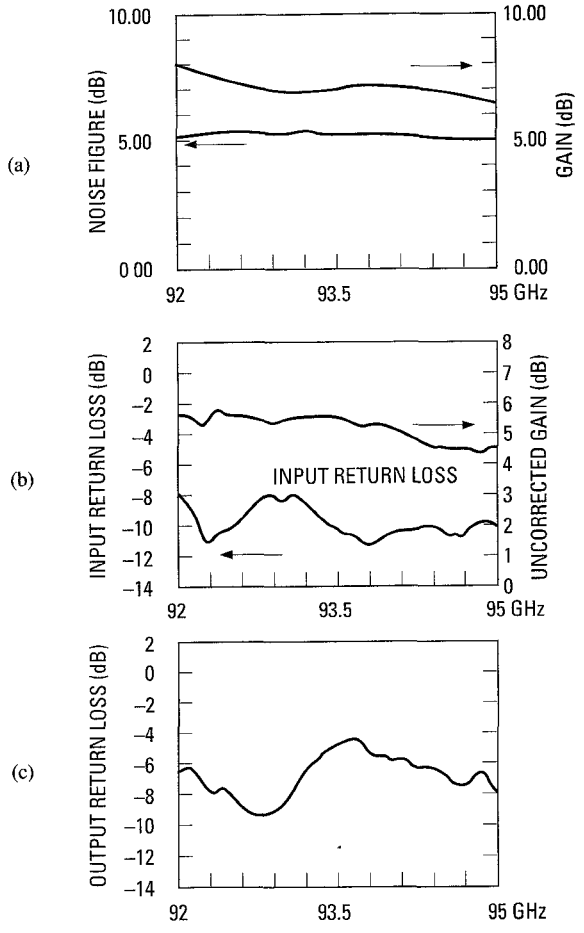


Fig. 10. Measurement results of the W-band one-stage MMIC LNA at 3 V drain bias. (a) Noise figure and associated small signal gain. (b) Input return loss and uncorrected gain. (c) Output return loss.

To demonstrate the effectiveness of our rigorous design/analysis methodology, a comparison of simulated two-stage LNA performance versus measurement under 2 V drain bias with gate biased near g_m peak condition is shown in Fig. 12(a)–(b). Fig. 12(a) presents the gain and input return loss, while Fig. 12(b) indicates the output return loss and noise figure. The gain agreement between measurement and simulation is within 1 dB from 80 to 100 GHz and noise figure agreement is better than 0.5 dB from 91 to 95 GHz. It is noted from Figs. 11(a) and 12(a) that the gain of this two-stage LNA for 2 V drain voltage is about 1.5 dB lower than that for 3 V condition, but the noise figure remains virtually unchanged.

The two-stage LNA has also been tested under different temperature conditions. Fig. 13 shows the gain and output power variation versus input power at $-35°C$, 23°C, and 65°C, respectively. The gain variation over temperature is less than 3 dB which approximates a temperature slope of -0.03 dB/°C, and the saturated output power variation is about 1 dB. Temperature compensation may be needed for some system applications.

C. Eight-Stage Amplifier Results

Due to the low return loss of the amplifiers, the monolithic chips are easily cascaded to make an ex-

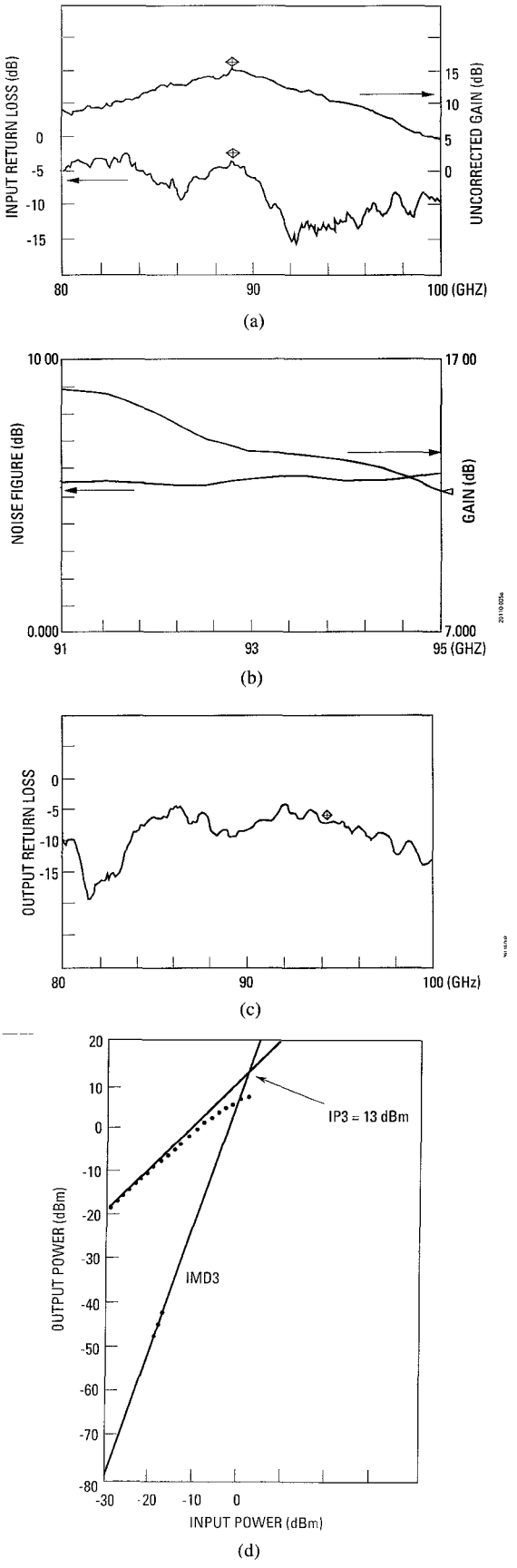


Fig. 11. Measurement results of the W-band two-stage MMIC LNA at 3 V drain bias. (a) Noise figure and associated small signal gain. (b) Input return loss and uncorrected gain. (c) Output return loss (d) P_{in} versus P_{out} and third harmonic intermodulation.

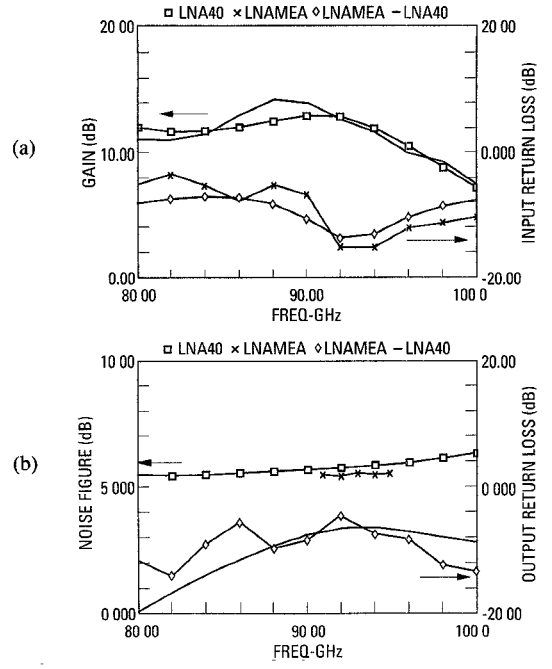


Fig. 12. Comparison between simulation (LNA40) and measurement (LNAMEA) of the two-stage LNA performance at 2 V drain bias condition. (a) Gain and input return loss. (b) Output return loss and noise figure.

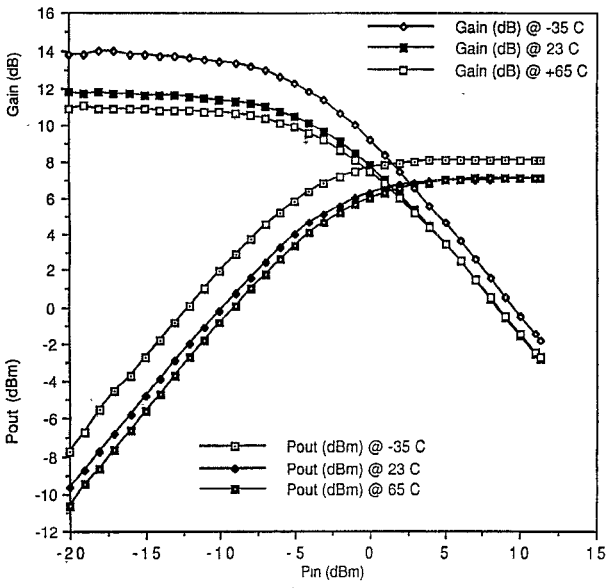


Fig. 13. Gain and output power performance variation of the two-stage LNA due to temperature.

tremely high gain amplifier suitable for some system applications. An eight-stage amplifiers has been successfully built using four monolithic two-stage LNA chips. Edge coupled lines fabricated on fused silica substrate are used to connect the monolithic chips and provide dc block. Detailed design information is described elsewhere [15]. The measured results were excellent. A noise figure of 6.5 dB with associated gain of 49 dB from waveguide to waveguide was achieved at 94 GHz. The schematic diagram of this eight-stage amplifiers and the measured noise

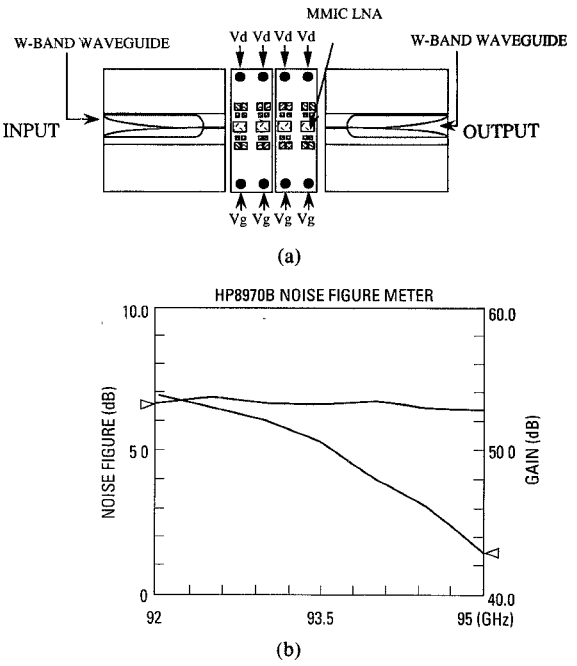


Fig. 14. The eight-stage *W*-band LNA. (a) Schematic diagram of the four cascaded monolithic two-stage amplifiers. (b) Gain and noise figure measurement of the complete unit from waveguide to waveguide (no correction is made).

figure with associated gain from 92–95 GHz are shown in Fig. 14.

The circuit yield of these monolithic chips has been excellent for the small sample tested. 20 LNA chips from the same three inch wafer were selected for testing simply by visual inspection. All of them are dc functional and only two of them do not show consistent RF performance. This high yield is attributed to stable MMIC process. The success of this eight-stage high gain amplifier is also ascribed to high yield of the monolithic two-stage LNA chips so that it was not difficult in obtaining enough functional chips on the same wafer to cascade the complete amplifier.

VI. Summary

We have presented recent development of *W*-band one- and two-stage PM HEMT monolithic LNA's. At 94 GHz, a gain of 13.3 dB and a noise figure of 5.5 dB, with a maximum gain of 17 dB at 89 GHz have been achieved for the two-stage LNA. The one-stage LNA also demonstrates a consistent performance of 5.1 dB noise figure with 7 dB associated gain. These encouraging results shows the potential of InGaAs PM HEMT technology for *W*-band high performance system applications, such as low noise receiver systems which require extremely high gain unit. The excellent device characteristics and rigorous design/analysis methodology are the foundations of this successful *W*-band monolithic IC design.

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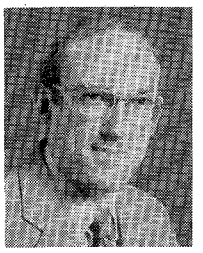

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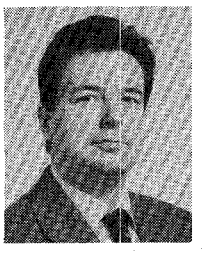

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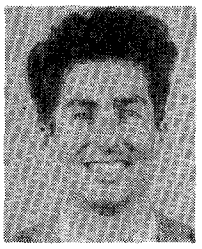

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